Kabeta Processor Design

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| Version: | Preliminary |
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| Reviewer: | (N/A) |

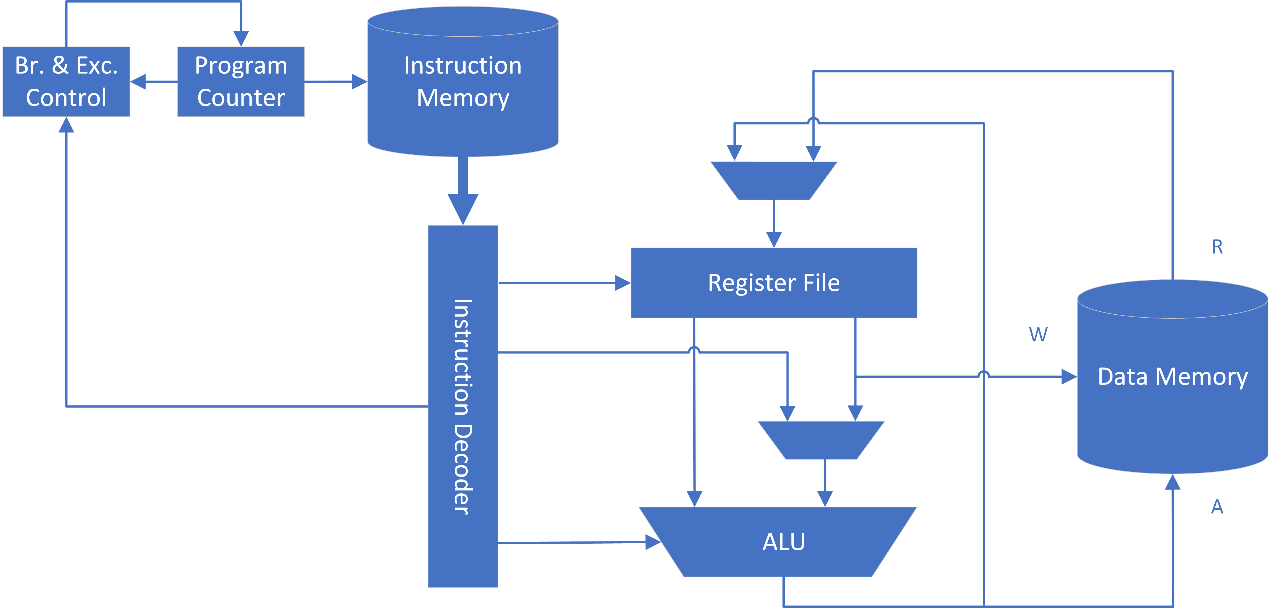
# Introduction

## Description

Kabeta is a RISC processor based on the β Processor of MIT. Its main features and limitations include:

* Typical 5-stage Pipeline with Bypass
* Supervisor and User Modes
* Separate Instruction and Data Space
* Single-cycle Synchronous on-chip RAM

## Components



Kabeta mainly consists of Register File, Arithmetic and Logic Unit, Instruction Registers and Decoders, Branch and Exception Control, Program Counter, on-chip Data Memory and Instruction Memory.

## Block Diagram

[Click Here to Open Detailed Block Diagram](Design%20Diagrams%20-%20Detailed%20Block%20Diagram.png)

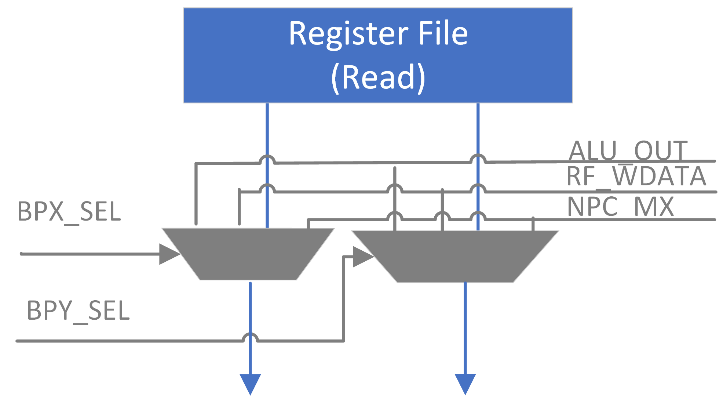
**IMPORTANT NOTE:** ALU in the diagram should contain an **output register**.

## References

* [MIT β Processor Specification](MIT6_004s09_lab_beta_doc.pdf)
* [MIT β Processor Summary](MIT6_004s09_lab_beta_summary.pdf)
* [Lecture Notes](https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-004-computation-structures-spring-2009/lecture-notes/) of [MIT 6.004 Computation Structures](https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-004-computation-structures-spring-2009/) ([L14](MIT6_004s09_lec14.pdf), [L22](MIT6_004s09_lec22.pdf), [L23](MIT6_004s09_lec23.pdf))

# Bypass

## Bypass Paths



## Control Signals

BPX\_SEL: (IR\_EX.Opcode in {OP, OPC, LD, ST, JMP, B\*}) // Instrns Read Ra

&& (IR\_EX.Ra != 31)

ALU\_OUT\_SELX : (IR\_EX.Ra == IR\_MX.Rc) && (IR\_MX.Opcode in {OP, OPC})

NPC\_MX\_SELX : (IR\_EX.Ra == IR\_MX.Rc) && (IR\_MX.Opcode in {JMP, B\*})

RF\_WDATA\_SELX : (!ALU\_OUT\_SELX && !NPC\_MX\_SELX) && (IR\_EX.Ra == IR\_WB.Rc) && (IR\_WB.Opcode in {OP, OPC, LD, LDR, JMP, B\*})

BPY\_SEL: (IR\_EX.Opcode in {OP}) // Instrns Read Rb

&& (IR\_EX.Rb != 31)

ALU\_OUT\_SELY : (IR\_EX.Rb == IR\_MX.Rc) && (IR\_MX.OpCode in {OP, OPC})

NPC\_MX\_SELY : (IR\_EX.Rb == IR\_MX.Rc) && (IR\_MX.Opcode in {JMP, B\*})

RF\_WDATA\_SELY : (!ALU\_OUT\_SELY && !NPC\_MX\_SELY) && (IR\_EX.Rb == IR\_WB.Rc) && (IR\_WB.Opcode in {OP, OPC, LD, LDR, JMP, B\*})

# Pipeline Stall

# Exception